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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/650,196 | 08/26/2003 | Huan-Ping Su | MM4635 | 6273 |

7590 05/05/2004

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| EXAMINER | |
|---|---|
| NADAV, ORI | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 10/650,196 | Applicant(s) SU, HUAN-PING | |
|---|---|---|---|
| | Examiner ori nadav | Art Unit 2811 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/26/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Sp cification*

The disclosure is objected to because of the following informalities: On page3, the phrase "FIG. 8" should read "FIG. 7".

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support in the disclosure and in the drawings for the claimed limitations of a plurality of conductive through vias used for electrically connecting the first chip to the first chip carrier via the second chip carrier and the conductive through vias, and a plurality of conductive traces used for electrically connecting the first chip to the first chip carrier via each of the conductive traces, as recited in claims 1 and 7, respectively.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitation of ",and an opposing non-active surface;", as recited in claims 1 and 7, is unclear as to which element the phrase refers.

The claimed limitations of conductive traces have one end connected to the ball pads of the second chip carrier and the other end connected to the ball pads of the first chip carrier, as recited in claim 12, are unclear as to which elements are the ball pads and their integration in the device.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asada (6,239,496) in view of Heo (6,555,917) and .Applicant Admitted Prior Art (AAPA). Asada teaches in figure 3B and related text a flip chip semiconductor package, comprising:

a first chip carrier substrate or TAB 113 (column 6, line 51) accommodating at least one first chip 133 having an active surface on which a plurality of inner leads 723 are formed for electrically connecting the first chip to the first chip carrier, and an opposing non-active surface;

a second chip carrier substrate 112 accommodating at least one second chip 132 having an active surface on which a plurality of inner leads 722 are formed for electrically connecting the second chip to the second chip carrier, and an opposing non-active surface;

the second chip of the second chip carrier is attached to the first chip of the first chip carrier;

a resin encapsulating layer 141-144, filled in between the first chip carrier and the second chip carrier for encapsulating the first chip, the second chip, and the plurality of inner leads; and a plurality of conductive through vias 251-253 extending axially between the first chip carrier, the resin encapsulating layer, and the second chip carrier for electrically connecting the first chip to the first chip carrier via the second chip carrier and the conductive through vias.

Asada does not teach using solder bumps and an adhesive layer to attach the second chip to the first chip.

Asada teaches in the embodiment of figure 8B and related text using solder balls instead of inner leads.

AAPA teaches on page 3 the advantages of using solder balls instead of inner leads.

Heo teaches in figure 8A and related text using an adhesive layer 28 to attach the second chip 10-3 to the first chip 10-2.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use solder bumps instead of inner leads and an adhesive layer to attach the second chip to the first chip in Asada's device, in order to improve the reliability of the device and to provide better bonding between the two chips, respectively. The combination is motivated by the teachings of AAPA which point out the advantages of using solder balls (page 3).

Regarding claim 2, Asada teaches in figure 8A a plurality of solder bumps are disposed on the exposed surface of the second chip carrier for forming electrical connection with another semiconductor package.

Regarding claims 5 and 10, Heo teaches in figure 8A an adhesive layer 28 being an insulating adhesive having high elasticity.

Regarding claim 6 and 11, Asada teaches in figure 3A and related text a resin encapsulating layer 141-144 being made of resin materials having low hygrosocopicity and low viscosity.

Regarding claim 7, Asada teaches in figure 3A and related text a plurality of conductive traces 121-124, 721-723 formed between the first chip carrier, the resin encapsulating

layer, and the second chip carrier for electrically connecting the first chip to the first chip carrier via each of the conductive traces.

Regarding claim 8, Asada teaches in figure 3A and related text conductive traces have one end connected to the ball pads 153 of the second chip carrier and the other end connected to the ball pads 152 of the first chip carrier.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References C-D are cited as being related to stacked chips having a through-hole.

**Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.**

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
4/27/04

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800